CLAIMS:

1. A data processing apparatus, comprising

- a register file with access ports;
- a functional unit coupled to the access ports for receiving operands,
- an instruction issue unit for issuing successive instructions from a program, the instruction issue unit being coupled to the access ports for selecting registers from which to read the operands specified in the instructions, the functional unit being arranged to start execution of a computation in response to reception of a first one of the instructions, a register in the register file for reading at least one of operands used in said computation being specified in a second one of the instructions issued by the instruction issue unit after issuing the first one of the instructions, the functional unit being arranged to suspend execution of the computation until after issue of the second one of the instructions when the second one of the instructions is not executed within a predetermined number of instruction cycles after the reception of the first one of the instructions.

2. A data processing apparatus according to Claim 1, wherein each instruction comprises an operation code, the functional unit being arranged to detect the operation code of instructions issued from the instruction issue unit to the functional unit, and to suspend execution of the computation specified by the first one of the instructions until after detection of an operation code that identifies the second one of the instructions.

3. A data processing apparatus according to Claim 2, wherein each of the instructions contains a field for an operand register selection code, the functional unit supplying a content of said field to the access port irrespective of the operation code.

4. A data processing apparatus according to Claim 2, wherein the functional unit selects an order in which steps of the computation are executed dependent on the operation code.

5. A data processing apparatus according to Claim 1, the second one of the instructions specifying a signal register in said register file, the functional unit being arranged to receive a signal from the specified signal register in response to the second one of the instructions, the functional unit suspending the computation unless the signal has a predetermined value indicating that the at least one of the operands is valid.

6. A data processing apparatus according to Claim 1, the functional unit being arranged to write different parts of a result of the computation to the register file in response to respective further ones of the instructions, each further one of the instructions specifying a register in the register file for writing its part of the result.

7. A data processing apparatus according to Claim 6, wherein the respective further ones of the instructions each contain an operation code and at least one reference to a register in the register file for writing one of the parts of the result, the functional unit selecting an order in which steps of the computation are executed dependent on a sequence in which the operation codes are received.

8. A data processing apparatus according to Claim 6, the further ones of the instructions each specifying a result part register and a signal register in said register file, the functional unit being arranged to output the result part and a signal to the result part register and the signal register respectively, at a predetermined time relative to reception of the further instruction, the functional unit being arranged to determine whether the result part required for the further instruction is available at said time, the functional unit indicating in said signal whether or not the result part is available at said time.